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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,006	09/11/2003	Joel Gerard Goodwin	AUS920030060US1	5933

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EXAMINER	
TABONE JR, JOHN J	
ART UNIT	PAPER NUMBER
2138	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/660,006	GOODWIN ET AL.	
	Examiner	Art Unit	
	John J. Tabone, Jr.	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

GUY LAMARRE
PRIMARY EXAMINER

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *09112003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 are pending and have been examined.

Specification

2. The disclosure is objected to because of the following informalities: On page 2, line 8, "and memory module, is presented" should be "and memory module is presented,". Delete comma after module and add comma after presented.

Appropriate correction is required.

Claim Objections

3. Claims 1, 14 and 25 are objected to because of the following informalities: In phrase "a memory card, said memory card,", "said memory card," is redundant and should be removed. Appropriate correction is required.

4. Claim 13 is objected to because it appears that this claim should be dependent on claim 2 and not claim 12. Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

5. Claims 25-27 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. These claims recite a computer program

product in a data processing system, but are not stored on a tangible computer readable medium.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1, 14 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Cox, (US-5357621), hereinafter Cox.

Claims 1, 14 and 25:

Cox teaches a memory system (**MCL system, Fig. 1**) includes a plurality of components, said plurality of components including a physical memory module (**memory block 1, Fig. 1**) coupled to a memory card (**memory module 20, Fig. 1**), said memory card, and a memory controller (**MCL Controller 13, Fig. 1**) for controlling said memory card, and logic (**MCL System Controller 11, Fig. 1**) that tests each one of said plurality of components separately to identify a defective one of said plurality of components. (Col. 3, ll. 23-27, col. 4, ll. 58-62, col. 10, l. 60 to col. 11, l. 7).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2-13, 15-24 and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cox, (US-5357621), hereinafter Cox, in view of James et al. (US005343478), hereinafter James.

Claims 2, 15 and 26:

Cox teaches logic that tests said physical memory module, logic that tests said memory card and that tests said memory controller. (Col. 4, ll. 37-62). However, Cox does not teach the specific order of the testing (i.e. in response to said physical memory module passing said test, etc.). James teaches in an analogous art using a serial bus (JTAG) to test components of a computer system and enable direct access to these components, even at the module level, using a modified JTAG configuration. (Abstract, col. 1, ll. 35-46, col. 8, ll. 56-62). James also teaches using the serial bus to shift test instructions into the modules for testing each module, which is illustrated in Fig. 13 and the discussed in cols. 12-13. With this, one skilled in the art can shift test data to test an individual module in any order desired. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Cox's serially connected memory test system (**MCL System Controller 11, MCL Controller 13, memory block 1 and 2, memory module 20**) to include James' modified JTAG bus and TAP controllers. The artisan would be motivated to do so because it would enable Cox to test the components of the memory stem in any desired order. Therefore, the specific order in claim 2, 15 and 26 would an obvious design choice.

Claims 3, 16 and 27:

Cox in view of James teaches said memory card including a buffer and wherein said step of testing said memory card includes: treating said buffer as a virtual memory module; and testing said memory card utilizing said virtual memory module as an obvious design choice as per the combination as per the rejection of claims 2, 15 and 26.

Claims 4 and 24:

Cox in view of James teaches said memory card including a buffer; and wherein said step of testing said physical memory module includes: treating said buffer as a virtual memory controller; and testing said physical memory module utilizing said virtual memory controller as an obvious design choice as per the combination as per the rejection of claims 2, 15 and 26.

Claims 5 and 17:

Cox in view of James teaches said memory card including a buffer; and wherein said step of testing said memory card includes: treating said buffer as a virtual memory module; and testing said memory card utilizing said buffer by writing a data pattern to said memory card to be stored in said virtual memory module; said step of testing said memory card including: storing said data pattern in said virtual memory module; reading a data pattern from said virtual memory; comparing said data pattern written to said virtual memory module to said data pattern read from said virtual memory module; determining that said memory card passed said test in response to said data pattern written to said virtual memory module being the same as said data pattern read from

said virtual memory module; and determining that said memory card failed said test in response to said data pattern written to said virtual memory module being different from said data pattern read from said virtual memory module as an obvious design choice as per the combination as per the rejection of claims 2, 15 and 26.

Claims 6 and 18:

Cox in view of James teaches said memory card including a plurality of buffers (**Modules 1-n 20, Fig. 1**) and assigning a unique identifier (**JTAG device ID, James – col. 13, ll. 53-65**) to each one of said plurality of buffers for addressing said plurality of buffers.

Claims 7, 8, 19 and 20:

Cox in view of James teaches coupling said buffer to a service processor (Cox - **MCL System Controller 11**, **James – CAT controller 102**), utilizing a JTAG bus, as per claims 8 and 20, and testing, utilizing said service processor, said memory card (**module 1 20**).

Claims 9 and 21:

Cox in view of James teaches storing a data pattern in said memory controller; reading a data pattern from said memory controller; comparing said data pattern written to said memory controller to said data pattern read from said memory controller; determining that said memory controller passed said test in response to said data pattern written to said memory controller being the same as said data pattern read from said memory controller; and determining that said memory controller failed said test in response to said data pattern written to said memory controller being different from said

data pattern read from said memory controller. (Cox - Col. 10, l 60 to col. 11, l. 7, claim 3).

Claims 10, 11 and 22:

Cox in view of James teaches said memory controller (**MCL Controller 13**) being coupled to a service processor (**MCL System Controller 11**) utilizing a JTAG bus (**TDI to TDO,** as per the combination as per the rejection of claims 2, 15 and 26).

Claims 12 and 23:

Cox in view of James teaches said memory card including a tristate device; and wherein said logic that tests said memory card includes: said tristate device acting as a virtual memory module; and logic that tests said memory card utilizing said virtual memory module as an obvious design choice as per the combination as per the rejection of claims 2, 15 and 26.

Claim 13:

Cox in view of James teaches said memory card including a tristate device; and wherein said step of testing said memory card includes: treating said tristate device as a virtual memory module; and testing said memory card utilizing said virtual memory module by writing a data pattern to said memory card; said step of testing said memory card including: storing said data pattern in said tristate device; reading a data pattern from said tristate device; comparing said data pattern written to said tristate device to said data pattern read from said tristate device; determining that said memory card passed said test in response to said data pattern written to said tristate device being the same as said data pattern read from said tristate device; and determining that said

memory card failed said test in response to said data pattern written to said tristate device being different from said data pattern read from said tristate device as an obvious design choice as per the combination as per the rejection of claims 2, 15 and 26.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to John J. Tabone, Jr. whose telephone number is (571) 272-3827. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

John J. Tabone, Jr. 3/27/07
Examiner
Art Unit 2138